Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

B.E/B.TECH DEGREE END SEMESTER THEORY EXAMINATIONS, NOV/DEC 2025

Fifth Semester

Electronics and Communication Engineering

CEC369 – IOT Processors

Regulations - 2021

Duration : 3 Hrs *Maximum : 100 Marks*

*PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)*

Q.No	*Questions*	*BTL*	*CO*	*Marks*
1.	Compare the Main Stack Pointer (MSP) and the Process Stack Pointer (PSP).	L2	1	2
2.	Differentiate the I-Code bus and D-Code bus based on their functions in the Cortex-M3 processor.	L2	1	2
3.	What is the main function of NVIC?	L1	2	2
4.	State late arrival in interrupt processing.	L1	2	2
5.	Give the advantage of using C for Cortex-M3/M4 programming.	L1	3	2
6.	Recall the default location of the vector table in Cortex-M3/M4.	L2	3	2
7.	Mention the role of GPIOs in STM32L15XXX.	L2	4	2
8.	Define USART.	L1	4	2
9.	Outline the importance of system level interconnection.	L2	5	2
10.	Identify die area.	L1	5	2

*PART – B (ANSWER ALL QUESTIONS) (Marks 5*16 = 80)*

Q.No		*Questions*	*BLT*	*CO*	*Marks*
11.	a	Explain in detail about the evolution of ARM architecture versions and discuss their significant features.	L2	1	16
		Or			
	b	Draw the detailed block diagram of the Cortex-M3 processor system and analyze the function of each block.	L2	1	16
12.	a	Discuss the various types of fault exceptions in the Cortex-M3 processor.	L2	2	16
		Or			
	b	Explain nested interrupts and tail-chaining interrupts with suitable diagrams and examples.	L2	2	16
13.	a	Describe exception programming using interrupts in Cortex-M3/M4.	L2	3	16
		Or			
	b	Explain the procedure for setting up the MPU with an example.	L2	3	16

14.	a	Outline the memory and bus architecture of STM32L15XXX with a neat diagram.	L2	4	16
		Or			
	b	Summarize the significance of software development tools cross assembler, compiler and debugger.	L2	4	16
15.	a	Develop the main components of a system architecture and their roles in a typical SoC.	L3	5	16
		Or			
	b	Construct the role of SoC design in image compression and video compression applications.	L3	5	16